Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A bit error rate tester that tests the bit error rate of a data transmission through an interface within a programmable logic device, the bit error rate tester comprising:

a first memory storing test data;

a second memory storing comparison data;

transmission circuitry implemented using programmable logic circuitry of [[a]] the programmable logic device, the transmission circuitry coupled to the interface within the programmable logic device and to the first memory for communicating the test data to the interface; and

comparison circuitry implemented using programmable logic circuitry of the programmable logic device, the comparison circuitry coupled to the interface and to the second memory for receiving incoming data from the interface and comparing the incoming data to the comparison data.

2. (Original) The bit error rate tester of claim 1 further comprising control circuitry coupled to the transmission circuitry and to the comparison circuitry.

3. (Original) The bit error rate tester of claim 2 wherein the control circuitry is implemented in the programmable logic device using programmable logic circuitry.

4. (Currently amended) The bit error rate tester of claim [[3]] 2 wherein the control circuitry is a processor.

5. (Original) The bit error rate tester of claim 1 further comprising user equipment coupled to the programmable logic device.

6. (Original) The bit error rate tester of claim 5 wherein the user equipment comprises a personal computer.

7. (Original) The bit error rate tester of claim 1 wherein the transmission circuitry comprises formatting circuitry.

8. (Original) The bit error rate tester of claim 1 wherein the comparison circuitry comprises formatting circuitry.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Original) The bit error rate tester of claim 1 wherein the test data and the comparison data are the same.

13. (Currently Amended) A programmable logic device comprising programmable logic circuitry configured to:

communicate test data to an interface within the programmable logic device;

receive within the programmable logic device incoming data from the interface; and

compare the incoming data to comparison data in order to determine the bit error rate of the interface, wherein the interface is internal to the programmable logic device.

14. (Currently amended) A programmable logic device comprising programmable logic circuitry configured to implement a bit error rate tester for testing the bit error rate of data transmitted through an interface internal to the programmable logic device.

15. (Original) A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

16. (Original) The printed circuit board of claim 15 further comprising a memory mounted on the printed circuit board and coupled to the memory circuitry.

17. (Original) The printed circuit board of claim 16 further comprising processing circuitry mounted on the printed circuit board and couple to the memory circuitry.

18. (Original) A method for synchronizing a comparison of incoming values with comparison values in a bit error rate tester implemented in a programmable logic device, the method comprising:

(1) comparing an incoming value to a

comparison value corresponding to an address counter;

(2) if the incoming value matches the comparison value then increasing the address counter by one unit, otherwise increasing the address counter by two units; and

(3) repeating (1) and (2) until a predetermined condition is met.

19. (Original) The method of claim 18 wherein (3) comprises repeating (1) and (2) until a predetermined number of consecutive matches have occurred.

20. (Original) The method of claim 18 wherein the comparison values comprises a pattern of values and wherein (3) comprises repeating (1) and (2) until all values in the pattern of values are consecutively matched.

21. (Currently amended) The method of claim 18 further comprising:

when the predetermined condition is met:

[[(1)]] (4) comparing an incoming value to a comparison value corresponding to a second address counter;

[[(2)]] (5) increasing the second address

counter by one unit and if the incoming value does not match the comparison value then increasing a bit error counter by one; and

[[(3)]] (6) repeating ~~(1) and (2)~~ (4) and (5) until a predetermined condition is met.

22. (Currently amended) A method for testing the bit error rate of a data transmission through an interface using a bit error rate tester implemented in [[a]] the programmable logic device, the method comprising within the programmable logic device:

communicating test data to the interface;

receiving incoming data from the interface;

comparing the incoming data to comparison data in order to determine the bit error rate of the data transmission through the interface, wherein the interface is internal to the programmable logic device.

23. (Canceled)

24. (Canceled)

25. (Original) The method of claim 22 wherein the comparing the incoming data to the comparison data comprises synchronizing the incoming data to the comparison data.

26. (New) A bit error rate tester that tests the bit error rate of a data transmission through an interface within a programmable logic device, the bit error rate tester comprising:

a memory storing test data;

transmission circuitry implemented using programmable logic circuitry of the programmable logic device, the transmission circuitry coupled to the interface within the programmable logic device and to the memory for communicating the test data to the interface; and

comparison circuitry implemented using programmable logic circuitry of the programmable logic device, the comparison circuitry coupled to the interface and to the memory for receiving incoming data from the interface and comparing the incoming data to the test data.

27. (New) The bit error rate tester of claim 26 further comprising control circuitry coupled to the transmission circuitry and to the comparison circuitry.

28. (New) The bit error rate tester of claim 27 wherein the control circuitry is implemented in the programmable logic device using programmable logic circuitry.

29. (New) The bit error rate tester of claim 27 wherein the control circuitry is a processor.

30. (New) The bit error rate tester of claim 26 further comprising user equipment coupled to the programmable logic device.

31. (New) The bit error rate tester of claim 30 wherein the user equipment comprises a personal computer.

32. (New) The bit error rate tester of claim 26 wherein the transmission circuitry comprises formatting circuitry.

33. (New) The bit error rate tester of claim 26 wherein the comparison circuitry comprises formatting circuitry.